AMENDMENTS

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently Amended): A method ~~for forming a calibrated critical dimension test wafer~~ for process control ~~of sub-tenth micron polysilicon features~~ in an integrated circuit process comprising:

~~(a)~~ providing a wafer substrate;

~~(b)~~ forming a pad ~~oxide~~ layer on said wafer substrate;

~~(c)~~ ~~depositing~~ forming a metal layer on said pad ~~oxide~~ layer;

~~(d)~~ patterning said metal layer to form at least one metal plate in at least one region of said wafer substrate;

~~(e)~~ milling a plurality of substantially parallel trenches in said at least one metal plate ~~with a focused ion beam~~, thereby forming a critical dimension test array wafer; and

~~(f)~~ measuring the widths of said parallel trenches ~~and the spacings~~ therebetween, thereby calibrating said critical dimension test array wafer;

mounting and inserting said calibrated critical dimension test array wafer in a sample chamber of a process control scanning electron microscope;

calibrating said process control scanning electron microscope by measuring the widths of said trenches therebetween; and

using said process control scanning electron microscope to measure widths of lines on an in-process integrated circuit wafer.

2. (Currently Amended): The method of claim 1 wherein said pad ~~oxide~~ layer is silicon oxide thermally grown to a thickness of between about 50 and 200 nm.

3. (Original): The method of claim 1 wherein said metal layer is between about 400 and 1,000 nm thick.

4. (Original): The method of claim 1 wherein said metal layer is an alloy of aluminum and copper wherein the copper content is between about 0.1 and 1.0 percent by weight.

5. (Currently Amended): The method of claim 16 wherein said ion are germanium.

6. (Currently Amended): The method of claim 16 wherein said ion beam has an energy of between about 25 and 35keV and a current of between about 0.5 and 3 pA.

7. (Original): The method of claim 1 wherein said trenches are between about 30 and 90 nm wide and have a width uniformity 3-sigma of between 3.0 and 3.5 nm.

8. (Original): The method of claim 1 wherein said trenches have a mean value of width roughness of between about 3.0 and 3.7 nm and a mean value of edge roughness of between about 1.8 and 2.2 nm.

9. (Currently Amended): The method of claim 1 wherein said measuring is accomplished using a calibrated scanning electron microscope.

10. (Currently Amended): A method ~~for using a calibrated critical dimension test wafer~~ for process control ~~of sub-tenth micron polysilicon features~~ in an integrated circuit process comprising:

~~(a)~~ providing a ~~calibrated critical dimension test~~ wafer substrate having a plurality of substantially parallel trenches and spaces milled~~, with a focused ion beam,~~ in a metal plate formed over a pad ~~oxide~~ layer~~,~~ ~~and calibrated according to the process cited by claim 1~~ thereby forming a critical dimension test array wafer, and the widths of said parallel trenches and the spaces therebetween being measured thereby calibrating said critical dimension test array wafer;

~~(b)~~ mounting and inserting said calibrated critical dimension test array wafer in ~~the~~ a sample chamber of a process control scanning electron microscope;

~~(c)~~ calibrating said process control scanning electron microscope by measuring the widths of said trenches and the spaces therebetween; and

~~(d) after said calibrating,~~ using said process control scanning electron microscope to measure widths and ~~spacings~~ spaces of ~~polysilicon~~ lines on an in-process integrated circuit wafer.

11. (Currently Amended): The method of claim 10 wherein said pad ~~oxide~~ layer is silicon oxide thermally grown to a thickness of between about 50 and 200 nm.

12. (Original): The method of claim 10 wherein said metal plate is between about 400 and 1,000 nm thick.

13. (Original): The method of claim 10 wherein said metal plate is an alloy of aluminum and copper wherein the copper content is between about 0.1 and 1.0 percent by weight.

14. (Currently Amended): The method of claim ~~10~~18 wherein said focused ion beam comprises germanium ions.

15. (Currently Amended): The method of claim ~~10~~18 wherein said focused ion beam has an energy of between about 25 and 35keV and a current of between about 0.5 and 3 pA.

16. (New): The method of claim 1 wherein said substantially parallel trenches are formed by a focused ion beam.

17. (New): The method of claim 10 wherein said lines comprise polysilicon lines.

18. (New): The method of claim 10 wherein said substantially parallel trenches are formed by a focused ion beam.